Code.No: RR310401 | RR | SET-1

**III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010**
**DIGITAL IC APPLICATIONS**
**(ELECTRONICS AND COMMUNICATIONS ENGINEERING)**

**Time: 3hours** **Max.Marks:80**

**Answer any FIVE questions**
**All questions carry equal marks**

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1.a) What is static and dynamic power dissipation of a CMOS circuit . Distinguish between them and derive the expression for dynamic power dissipation.
b) Explain how one can estimate sinking current for low output and sourcing current for high output of CMOS gate. [8+8]

2.a) Explain the following terms with reference to TTL gate
i) DC Noise margin ii) FANOUT iii) Logic levels
b) Draw a neat transistor circuit of three input ECL NOR gate, and explain its operation. [8+8]

3.a) Write a VHDL code to model a 16:1 MUX using 'case' statement.
b) Design a carry loop ahead adder by using a dataflow model of VHDL code. [8+8]

4.a) Explain the internal structure of a $74\times157$ MUX.
b) Write a VHDL code in structural model to design the following Boolean function using $74\times157$ MUX
f = $A\overline{B}+AB\left(C+\overline{A}\right)$ [8+8]

5. Design a digital circuit which counts number of zero's in a 16 bit register. Write VHDL program in behavioral model to design this counter. [16]

6.a) What is meant by a synchronous counter? Design a modulo-8 synchronous circuit.
b) Explain the internal logic diagram of PAL 16R8. [8+8]

7.a) Define the terms clock skew? How does it effect the output of a synchronous circuit?
b) Design a 4 bit Johnson ring counter ( use a suitable IC In the design.) [8+8]

8.a) Explain and draw the general architecture of CPLD ? What are the key features of xilinx XC9500 CPLD?
b) With the help of timing waveforms, explain 'Read' and write operations of SRAM. [8+8]

**--ooOoo--**

Code.No: RR310401 | RR | SET-2

**III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010**
**DIGITAL IC APPLICATIONS**
**(ELECTRONICS AND COMMUNICATIONS ENGINEERING)**

**Time: 3hours** **Max.Marks:80**

**Answer any FIVE questions**
**All questions carry equal marks**

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[8+8]

1.a) Write a VHDL code to model a 16:1 MUX using 'case' statement.
b) Design a carry loop ahead adder by using a dataflow model of VHDL code. [8+8]

2.a) Explain the internal structure of a $74\times157$ MUX.
b) Write a VHDL code in structural model to design the following Boolean function using $74\times157$ MUX
f = $A\overline{B}+AB\left(C+\overline{A}\right)$ [8+8]

3. Design a digital circuit which counts number of zero's in a 16 bit register. Write VHDL program in behavioral model to design this counter. [16]

4.a) What is meant by a synchronous counter? Design a modulo-8 synchronous circuit.
b) Explain the internal logic diagram of PAL 16R8. [8+8]

5.a) Define the terms clock skew? How does it effect the output of a synchronous circuit?
b) Design a 4 bit Johnson ring counter ( use a suitable IC In the design.) [8+8]

6.a) Explain and draw the general architecture of CPLD ? What are the key features of xilinx XC9500 CPLD?
b) With the help of timing waveforms, explain 'Read' and write operations of SRAM. [8+8]

7.a) What is static and dynamic power dissipation of a CMOS circuit . Distinguish between them and derive the expression for dynamic power dissipation.
b) Explain how one can estimate sinking current for low output and sourcing current for high output of CMOS gate. [8+8]

8.a) Explain the following terms with reference to TTL gate
i) DC Noise margin ii) FANOUT iii) Logic levels
b) Draw a neat transistor circuit of three input ECL NOR gate, and explain its operation.

**--ooOoo--**

Code.No: RR310401 | RR | SET-3

**III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010**
**DIGITAL IC APPLICATIONS**
**(ELECTRONICS AND COMMUNICATIONS ENGINEERING)**

**Time: 3hours** **Max.Marks:80**

**Answer any FIVE questions**
**All questions carry equal marks**

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1. Design a digital circuit which counts number of zero's in a 16 bit register. Write VHDL program in behavioral model to design this counter. [16]

2.a) What is meant by a synchronous counter? Design a modulo-8 synchronous circuit.
b) Explain the internal logic diagram of PAL 16R8. [8+8]

3.a) Define the terms clock skew? How does it effect the output of a synchronous circuit?
b) Design a 4 bit Johnson ring counter ( use a suitable IC In the design.) [8+8]

4.a) Explain and draw the general architecture of CPLD ? What are the key features of xilinx XC9500 CPLD?
b) With the help of timing waveforms, explain 'Read' and write operations of SRAM. [8+8]

5.a) What is static and dynamic power dissipation of a CMOS circuit . Distinguish between them and derive the expression for dynamic power dissipation.
b) Explain how one can estimate sinking current for low output and sourcing current for high output of CMOS gate. [8+8]

6.a) Explain the following terms with reference to TTL gate
i) DC Noise margin ii) FANOUT iii) Logic levels
b) Draw a neat transistor circuit of three input ECL NOR gate, and explain its operation. [8+8]

7.a) Write a VHDL code to model a 16:1 MUX using 'case' statement.
b) Design a carry loop ahead adder by using a dataflow model of VHDL code. [8+8]

8.a) Explain the internal structure of a $74\times157$ MUX.
b) Write a VHDL code in structural model to design the following Boolean function using $74\times157$ MUX

f = $A\overline{B}+AB\left(C+\overline{A}\right)$ [8+8]

**--ooOoo--**

Code.No: RR310401 | RR | SET-4

**III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010**
**DIGITAL IC APPLICATIONS**
**(ELECTRONICS AND COMMUNICATIONS ENGINEERING)**

**Time: 3hours** **Max.Marks:80**

**Answer any FIVE questions**
**All questions carry equal marks**

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1.a) Define the terms clock skew? How does it effect the output of a synchronous circuit?
b) Design a 4 bit Johnson ring counter ( use a suitable IC In the design.) [8+8]

2.a) Explain and draw the general architecture of CPLD ? What are the key features of xilinx XC9500 CPLD?
b) With the help of timing waveforms, explain 'Read' and write operations of SRAM. [8+8]

3.a) What is static and dynamic power dissipation of a CMOS circuit . Distinguish between them and derive the expression for dynamic power dissipation.
b) Explain how one can estimate sinking current for low output and sourcing current for high output of CMOS gate. [8+8]

4.a) Explain the following terms with reference to TTL gate
i) DC Noise margin ii) FANOUT iii) Logic levels
b) Draw a neat transistor circuit of three input ECL NOR gate, and explain its operation. [8+8]

5.a) Write a VHDL code to model a 16:1 MUX using 'case' statement.
b) Design a carry loop ahead adder by using a dataflow model of VHDL code. [8+8]

6.a) Explain the internal structure of a $74\times157$ MUX.
b) Write a VHDL code in structural model to design the following Boolean function using $74\times157$ MUX

f = $A\overline{B}+AB\left(C+\overline{A}\right)$ [8+8]

7. Design a digital circuit which counts number of zero's in a 16 bit register. Write VHDL program in behavioral model to design this counter. [16]

8.a) What is meant by a synchronous counter? Design a modulo-8 synchronous circuit.
b) Explain the internal logic diagram of PAL 16R8. [8+8]

**--ooOoo--**